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Title:

LOW CAPACITANCE SELF-ALIGNED SEMICONDUCTOR ELECTRODE STRUCTURE AND METHOD OF FABRICATION ;

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Applicant(s): GTE LABORATORIES INC ;

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Equivalents: CA1167981, DE3150775, IT1142632, JP57130479 ;

ABSTRACT:

A semiconductor electrode structure with low parasitic capacitance is produced by a method for forming low capacitance first and second electrodes 34 24 in the semiconductor device, which may be a static induction transistor, while avoiding the requirement for precision mask alignment and mask to mask registration. During formation of electrode contacts, the first electrode 24 is protected by silicon nitride (22) and a low resistivity silicon layer (26) is grown over the semiconductor wafer, forming epitaxial regions (28) over the second electrodes (24) and a polycrystalline region (30) over protected portions of the wafer. The silicon layer is selectively etched by a mixture which removes the polycrystalline region (30) but does not appreciably affect the epitaxial regions (28). Second electrode metallic contacts are made in enlarged regions of the second electrodes where mask alignment is not critical. The reduction in contact window overlap by metallic contacts reduces parasitic capacitance.

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(58) Field of search
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(54) Low capacitance self-aligned semiconductor electrode structure and method of fabrication

(57) A semiconductor electrode structure with low parasitic capacitance is produced by a method for forming low capacitance first and second electrodes 34 24 in the semiconductor device, which may be a static induction transistor, while avoiding the requirement for precision mask alignment and mask to mask registration. During formation of electrode contacts, the first electrode 24 is protected by silicon nitride (22) and a low resistivity silicon layer (26) is grown over the semiconductor wafer, forming epitaxial regions (28) over the second electrodes (24) and a polycrystalline region (30) over protected portions of the wafer. The silicon layer is selectively etched by a mixture which removes the polycrystalline region (30) but does not appreciably affect the epitaxial regions (28). Second electrode metallic contacts are made in enlarged regions of the second electrodes where mask aligment is not critical. The reduction in contact window overlap by metallic contacts reduces parasitic capacitance.

FIG. 4

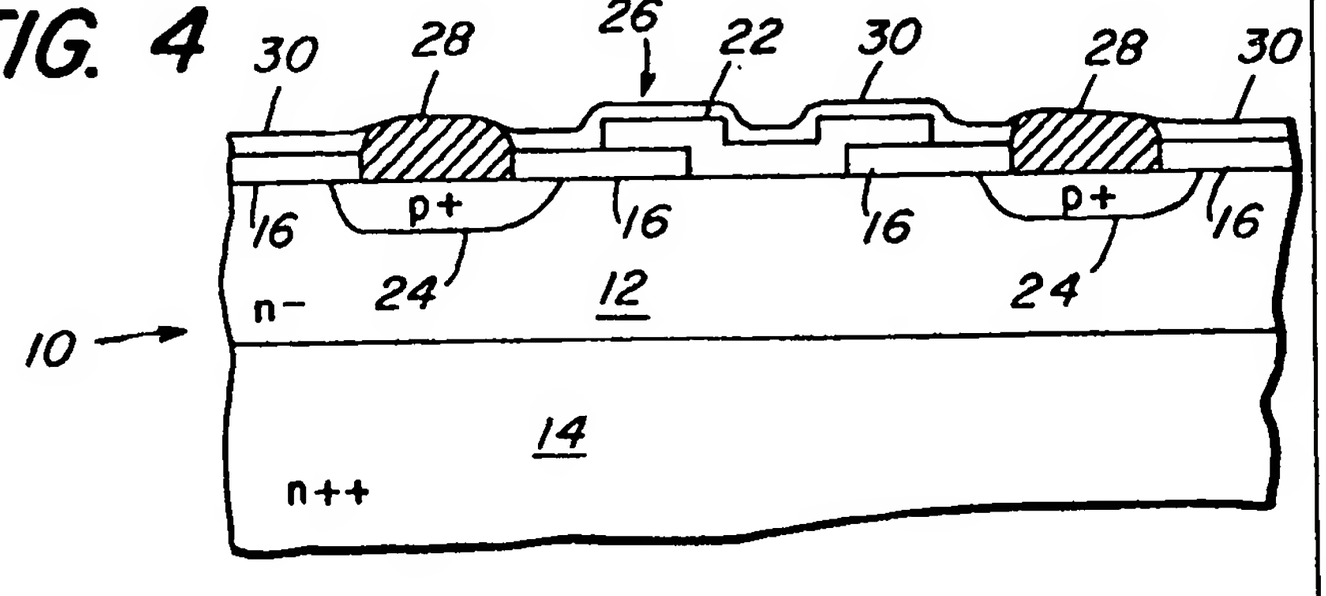
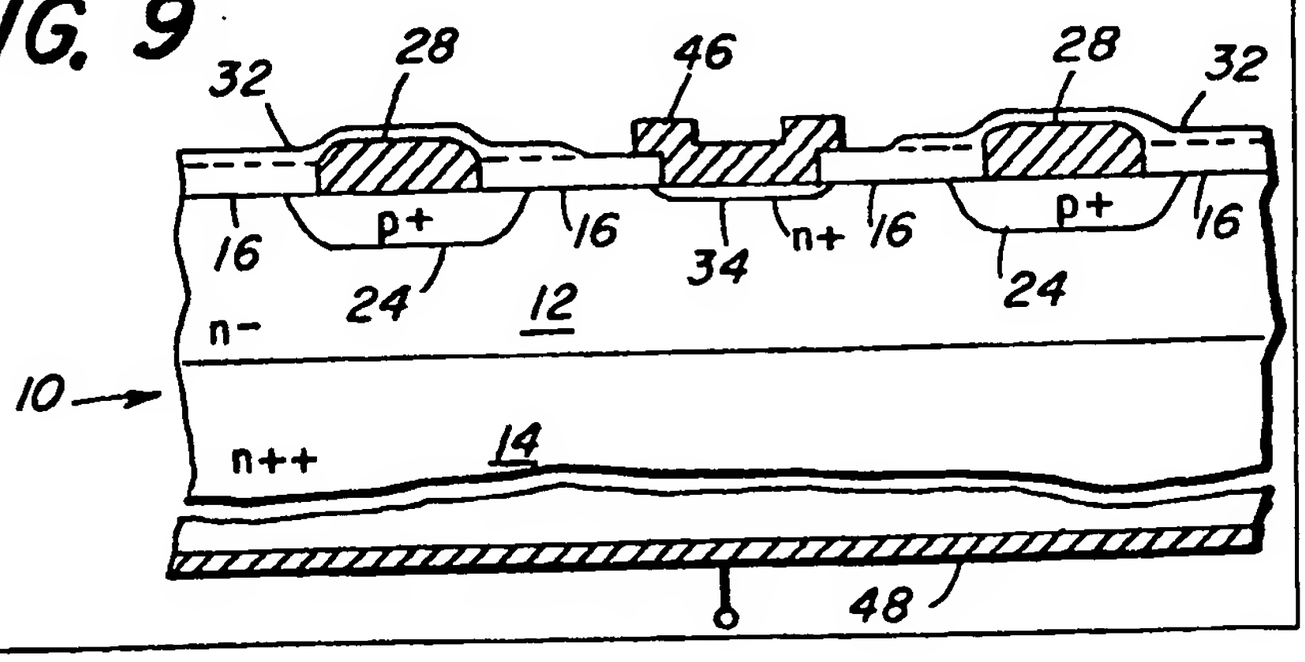


FIG. 9



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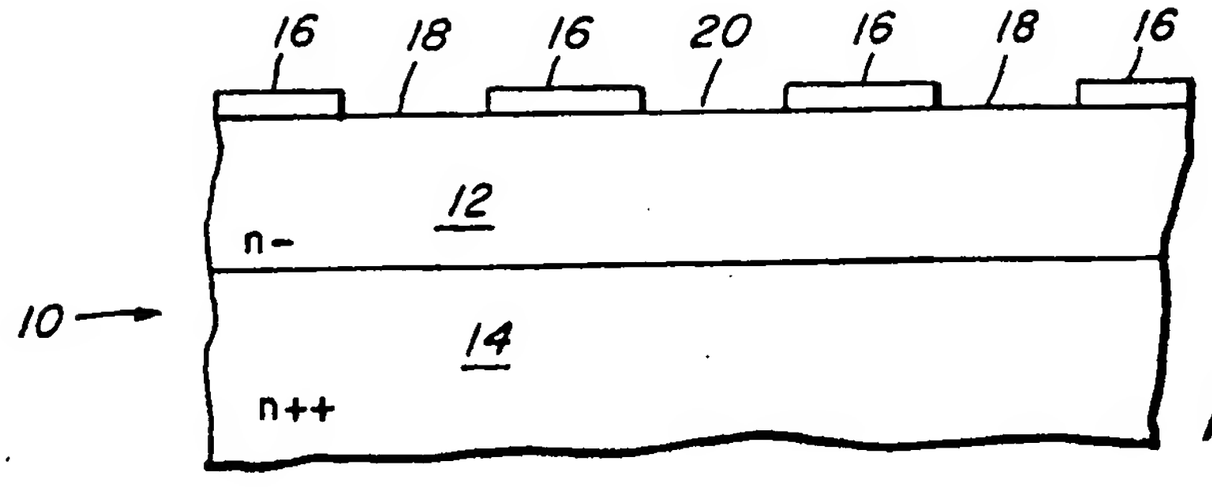

FIG. 1

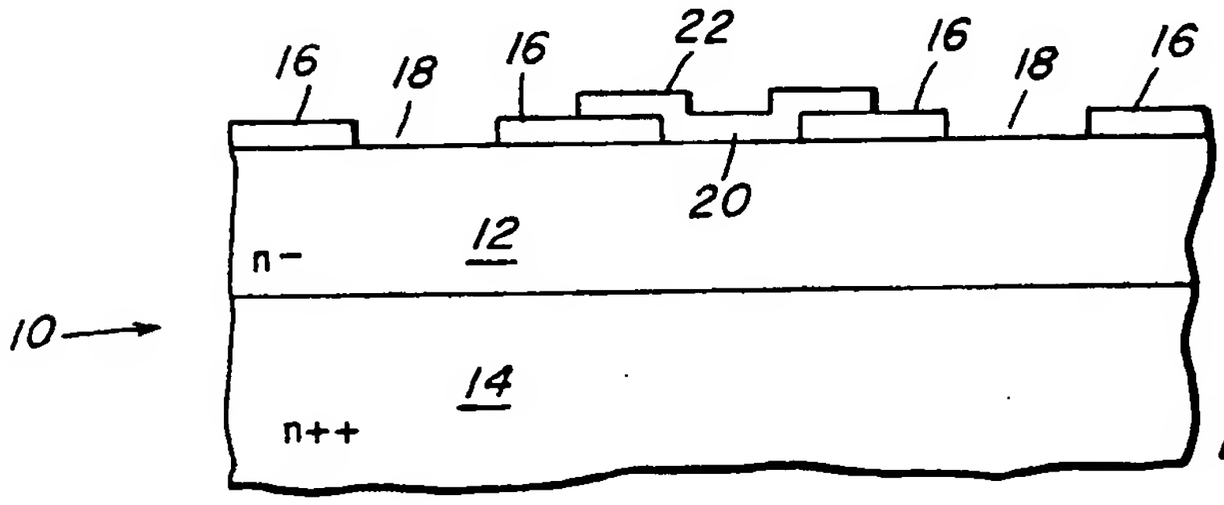

FIG. 2

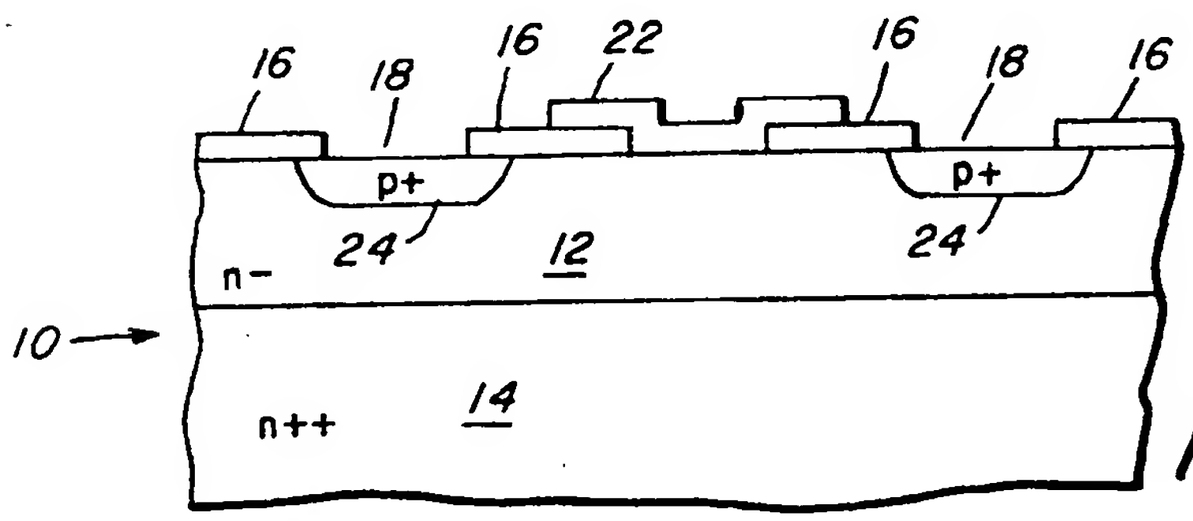

FIG. 3

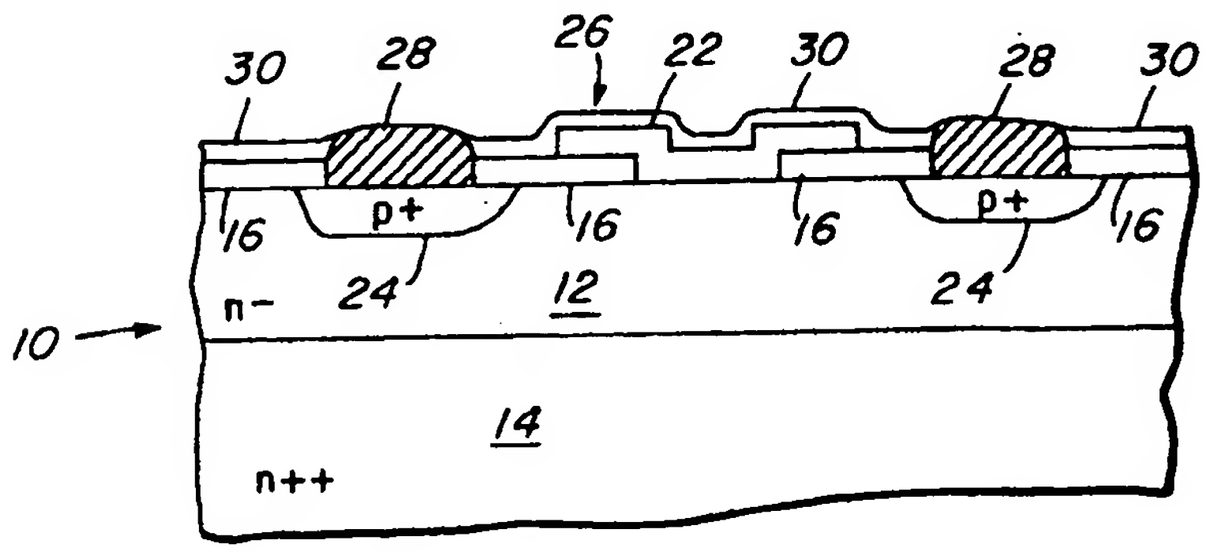

FIG. 4

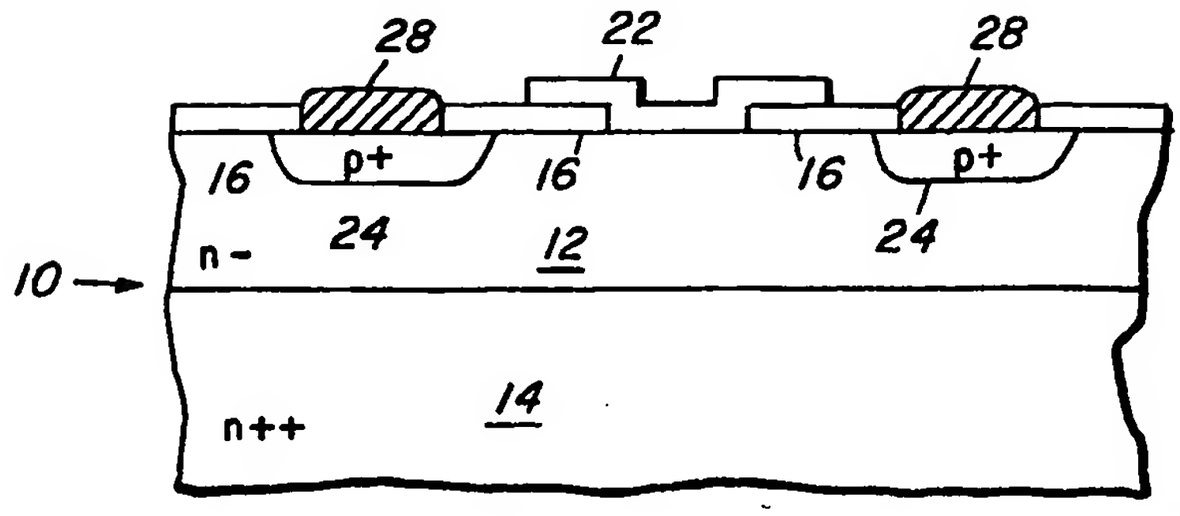

FIG. 5

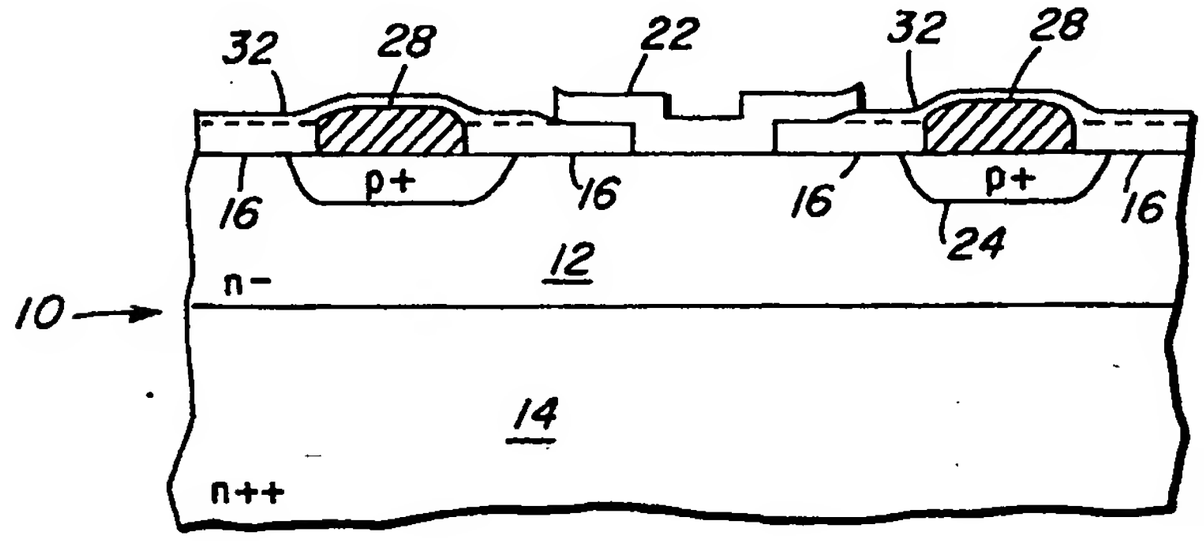

FIG. 6

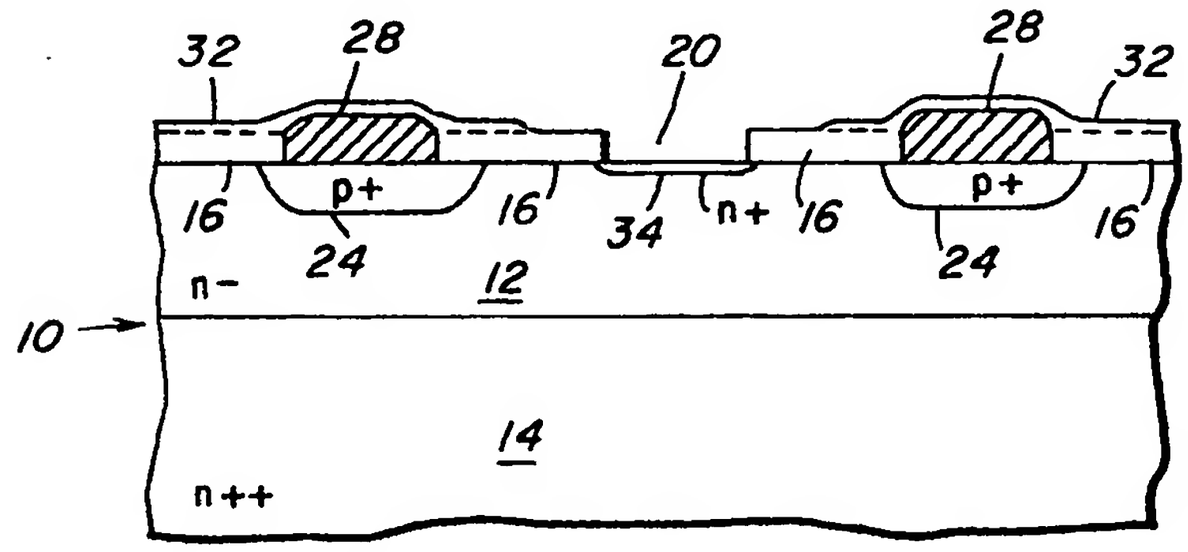

FIG. 7

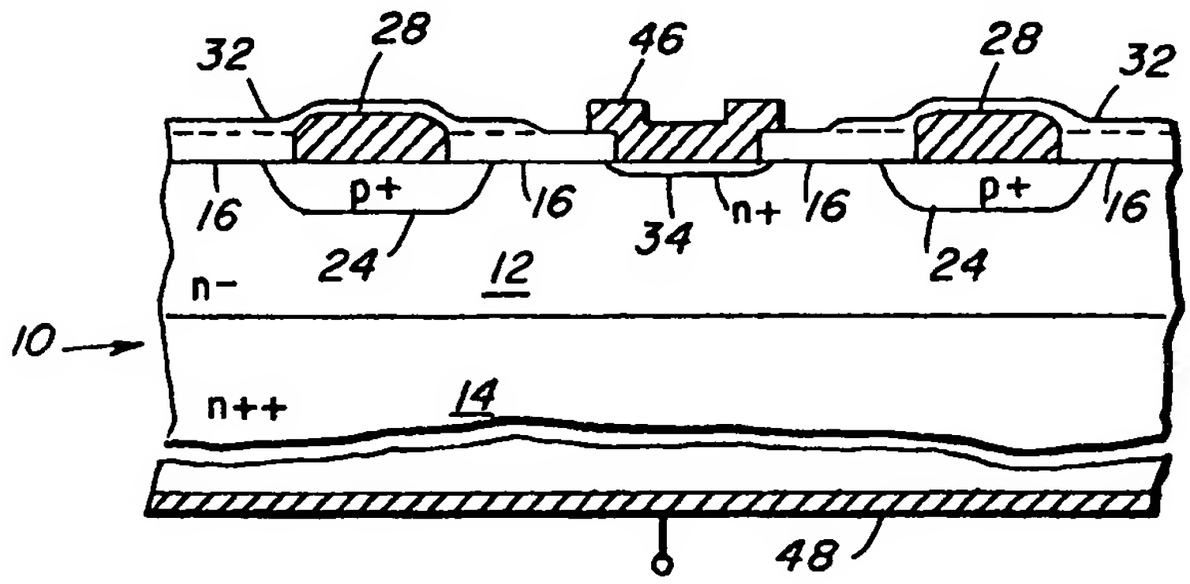

FIG. 9

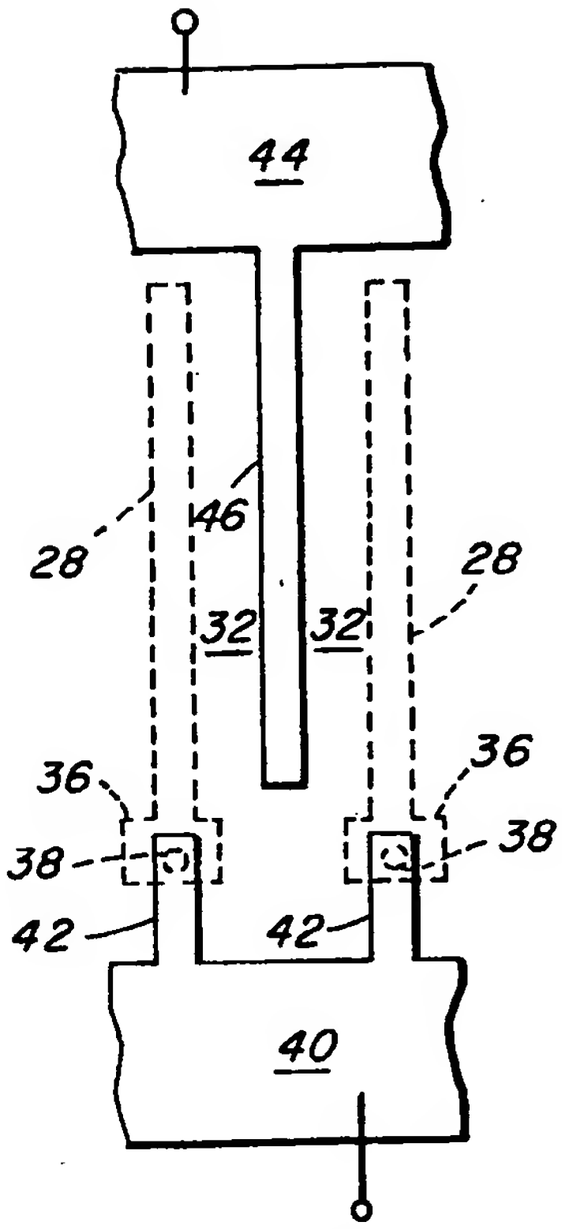

FIG. 8

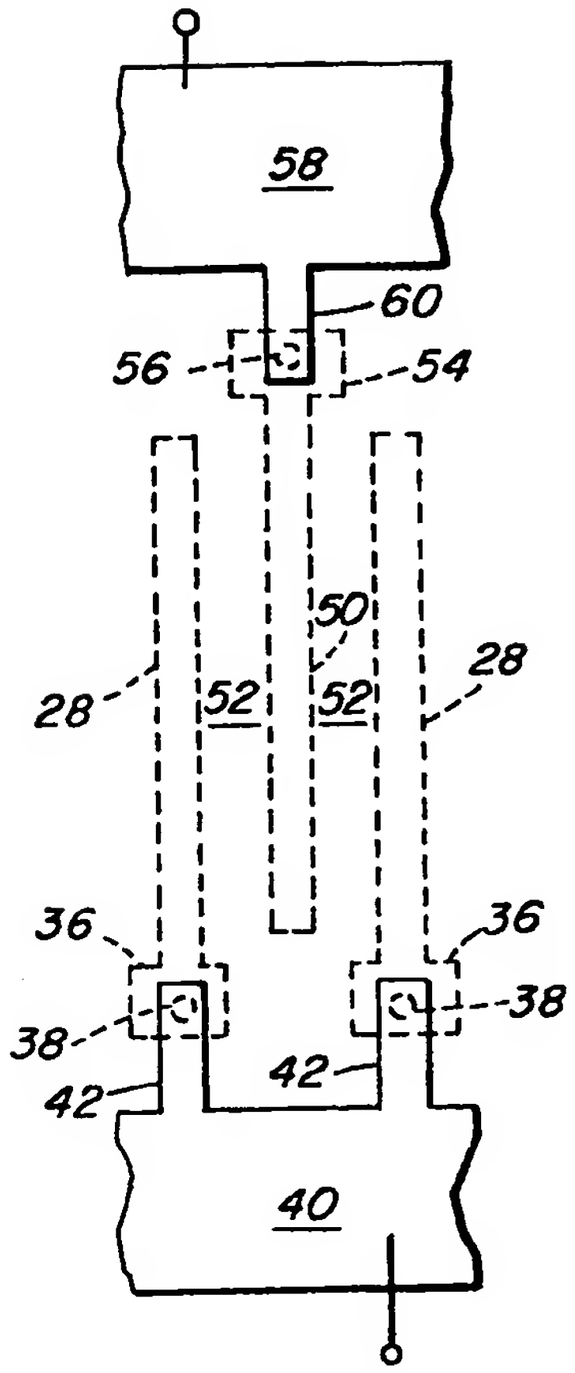

FIG. 11

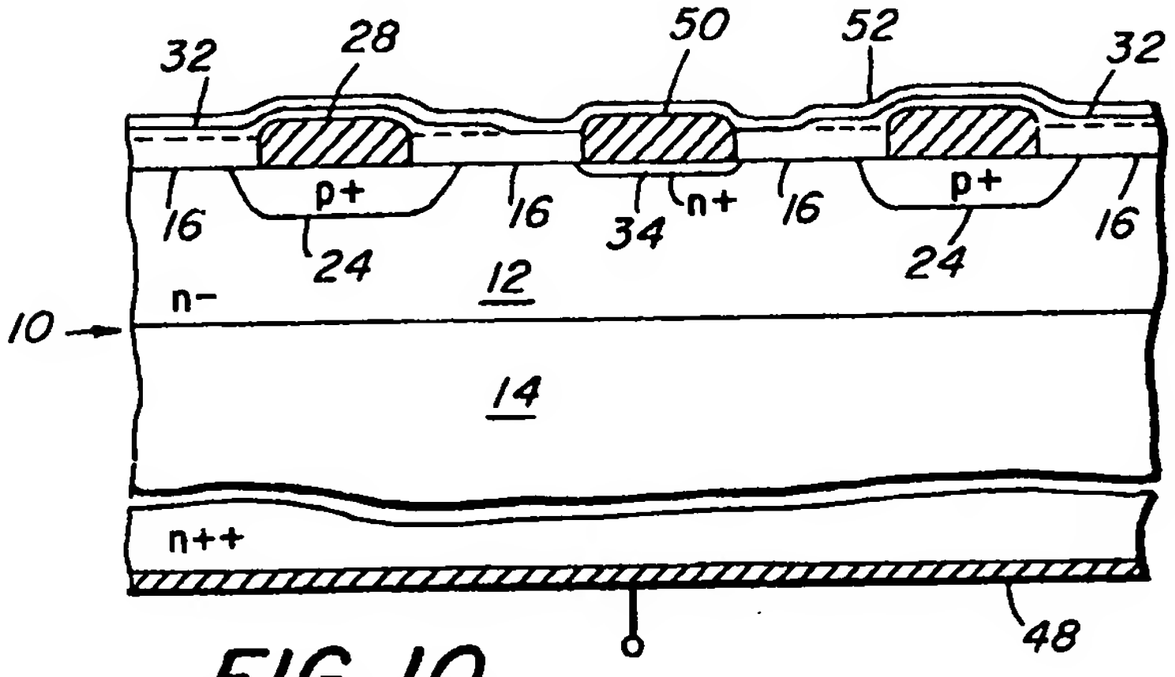

FIG. 10

SPECIFICATION

Low capacitance self-aligned semiconductor electrode structure and method of fabrication

This invention relates to high frequency semiconductor devices and, more particularly, to an electrode structure with low parasitic capacitance and a method for fabricating low capacitance electrodes in a semiconductor device while avoiding the requirement for precision mask alignment.

Semiconductor devices designed for high frequency operation require electrodes having extremely small dimensions and must be fabricated under extremely tight dimensional control to minimize stray capacitance and series resistance. Devices designed for operation at or above one gigahertz utilize electrode widths of one or two microns and electrode separations of a few microns. Photolithographic alignment and mask to mask registration, therefore, requires a precision of a few tenths of a micron. Such requirements make processing of high frequency semiconductor devices costly and difficult.

One example of a device requiring precision alignment and mask to mask registration is the static induction transistor, a field effect device which exhibits excellent high power and high frequency capabilities. The static induction transistor (SIT) typically utilizes a vertical geometry. Source and drain contacts are placed on opposite sides of a thin, high-resistivity layer of one conductivity type. Gate regions of the opposite conductivity type are diffused into the high resistivity layer on opposite sides of the source. Gate and source widths are typically 1.5 microns while the gate to source spacing is typically 5 microns. A slight mask misalignment can result in short-circuited semiconductor devices or can degrade device performance. Furthermore, the parasitic capacitance associated with metallic contact overlap degrades device performance. It is, therefore, desirable to provide an electrode structure in which the parasitic capacitance associated with metallic contact window overlap is reduced and to provide a method for fabricating low capacitance elecctrodes in semiconductor devices while avoiding the requirement for precision mask alignment and mask to mask registration.

According to the present invention there is provided a method for forming self-aligned first and second electrodes in a semiconductor device while avoiding the requirement for precision mask alignment and mask to mask registration. A first oxide layer is grown on a silicon semiconductor wafer in which the first and the second electrodes are to be formed. First and second windows are opened in the first oxide layer. A protective silicon nitride layer is deposited in the first window. The semiconductor wafer is doped with impurities through the second window, thereby forming the second electrode. A silicon layer of the same conductivity type as the second electrode is grown over the wafer. The silicon layer grows as a low resistivity monocrystalline region over the second electrode and as a polycrystalline region over the remainder of the wafer. The wafer is exposed to a first etching solution which removes the polycrystalline region but which has little effect on the monocrystalline region. A second oxide layer is grown on the wafer in a low temperature, high-pressure process. The wafer is then exposed to a second etching solution which removes the silicon nitride layer from the first window without affecting the oxide layers. The semiconductor wafer is doped with impurities through the first window thereby forming the first electrode. A contact window is opened through the second oxide layer to the monocrystalline region. Finally, metal is patterned and deposited over the contact window and the first electrode for making electrical contact to the first and second electrodes. The silicon layer is typically grown in an epitaxial reactor by chemical vapor deposition. One example of a semiconductor device to which the method of the present invention is applicable is the static induction transistor.

According to another aspect of the present invention, there is provided a field effect semiconductor device having low parasitic capacitance. The device includes a high resistivity layer of semiconductor material of one conductivity type with a low resistivity source electrode formed on a first surface thereof and a low resistivity drain electrode formed on a second surface thereof. Low resistivity gate electrodes of the opposite conductivity type are formed on the first surface of the high resistivity layer on opposite sides of the source electrode. Very low resistivity monocrystalline silicon gate contacts are disposed on the gate electrodes without overlap thereof. The gate contacts have the same conductivity type as the gate electrodes and include enlarged portions to which electrical contact is made by a gate metallization. The gate and source electrodes can have the form of parallel strips in the first surface of the high resistivity layer with the enlarged portions of the gate contacts located at one end of the parallel strips.

The invention is illustrated by way of example in the accompanying drawings, in which:—

Figure 1 is a cross-sectional view of a semiconductor wafer after opening of gate and source windows in a first oxide layer;

Figure 2 is a cross-sectional view of the semiconductor wafer of Fig. 1 after deposition of a silicon nitride layer in the source window;

Figure 3 is a cross-sectional view of the semiconductor wafer shown in Fig. 2 after doping of the gate electrodes;

Figure 4 is a cross-sectional view of the semiconductor wafer shown in Fig. 3 after growth of a silicon layer over the wafer;

Figure 5 is a cross-sectional view of the semiconductor wafer shown in Fig. 4 after etching of the polycrystalline portion of the silicon layer;

Figure 6 is a cross-sectional view of the semiconductor wafer shown in Fig. 5 after growth of a second oxide layer;

Figure 7 is a cross-sectional view of the semiconductor wafer shown in Fig. 6 after etching of the silicon nitride layer and doping of the source electrode;

Figure 8 is a top view of the semiconductor wafer shown in Fig. 7 after deposition and patterning of the source and gate metallizations;

Figure 9 is a cross-sectional view of the semiconductor wafer shown in Fig. 8;

Figure 10 is a cross-sectional view of the semiconductor wafer shown in Fig. 7 illustrating an alternative method of making electrical contact to the source electrode; and

Figure 11 is a top view of the semiconductor wafer shown in Fig. 10 illustrating the source and gate metallizations.

For a better understanding of the present invention together with other and further objects, advantages and capabilities thereof reference is made to the following disclosure and appended claims in connection with the above described drawings.

A method for forming self-aligned first and second electrodes in a semiconductor device while avoiding the requirement for precision mask alignment and mask to mask registration is described by way of example in connecton with a vertical geometry static induction transistor (SIT). The SIT includes source and drain electrodes on opposite sides of a thin, high-resistivity layer of one conductivity type and gate electrodes of the opposite conductivity type in the high resistivity layer on opposite sides of the source. For operation in the one gigahertz frequency range, it is necessary that the widths and spacing of the gate and source electrodes be on the order of a few microns.

Referring now to Fig. 1, there is shown a partial cross-sectional view of a semiconductor wafer 10. A high resistivity epitaxial layer 12 is grown on a highly doped substrate 14 of one conductivity type. In a typical device the substrate 14 provides mechanical support and is about 200 microns in thickness while the epitaxial layer 12 is about 7 to 10 microns in thickness and has a resistivity of at least 30 ohms centimeters. Next, a silicon dioxide layer 16 is grown on the upper surface of the epitaxial layer 12. The oxide layer 16 can be formed by known methods such as exposing the semiconductor wafer 10 to an oxygen and steam ambient at about 1100°C. Gate windows 18 and a source window 20 are formed in the oxide layer 16 in the next step. In a typical method of forming windows 18 and 20, a photoresist material is applied to the upper surface of the oxide layer 16, exposed through a patterned mask, and developed. The exposed portions of the oxide layer 16 are etched by a suitable solution such as buffered HF, or NH_4:HF, to form the windows 18 and 20. Since the gate windows 18 and the source window 20 are formed at the same time no alignment is required during this step.

Referring now to Fig. 2, the semiconductor wafer 10 is shown after deposition of a silicon nitride layer 22 in the source window 20 according to the next step of the process. A typical method of forming the silicon nitride layer 22 is by chemical vapor deposition from ammonia at about 800°C. While a mask is required for patterning the silicon nitride, precision alignment of the mask is not required. The dimension of the mask aperture is made larger than the dimension of the source window 20 so that the silicon nitride layer 22 overlaps the source window 20. Overlap of the silicon nitride layer 22 is not a problem as long as it does not extend into the gate windows 18. The silicon nitride layer 22 protects the high resistivity epitaxial layer 12 beneath the source window 20 during the succeeding steps of the process.

In the next step of the process the epitaxial layer 12 is doped through the gate windows 18 to form gate electrodes 24, as shown in Fig. 3. The gate electrodes 24 can be formed by standard methods of ion implantation and drive-in diffusion or by prediffusion and drive-in diffusion. In the example of the static induction transistor, the gate electrodes 24 have low resistivity and are of the opposite conductivity type from the epitaxial layer 12. This step requires no alignment.

The semiconductor wafer 10 is now introduced into an epitaxial reactor for growth of a silicon layer 26 over its top surface as shown in Fig. 4. The silicon layer 26 is grown by standard chemical vapor deposition techniques from a SiH_4-H_2 gas system at a temperature between about 950°C and 1000°C. In the growth of the silicon layer 26, monocrystalline, or epitaxial, regions 28 are formed in the gate windows 18 as a continuation of the crystal structure of the gate electrodes 24. A polycrystalline region 30 is formed over the remainder of the semiconductor wafer 10, including the oxide layer 16 and the silicon nitride layer 22. The monocrystalline regions 28 grow at a faster rate and become thicker than the polycrystalline region 30. Since the monocrystalline regions 28 act as the contacts to the gate electrodes 24, these regions are formed with the same conductivity type as the gate electrodes 24 and have low resistivity. In the present example, the monocrystalline regions 28 are grown to about 15,000 angstroms in thickness.

It is possible, by controlling the epitaxial growth conditions, to reduce the rate of growth of the undesired polycrystalline region 30. When the Si_4-H_2 gas system is used, growth temperatures of about 1200°C minimize growth of the polycrystalline region 30 on SiO_2. However, unacceptable impurity redistribution can occur in the semiconductor wafer 10 at 1200°C. Therefore, lower temperatures are preferred. As described hereinafter, the polycrystalline region 30 can be removed by etching techniques.

The silicon layer 26 can be alternatively be grown using a $SiCL_4$-HCl-H_2 gas system. The use of silicon chlorides with HCl was described by R. K. Smeltzer, in "Epitaxial Deposition of Silicon in Deep Grooves", J. Electrochem. Soc.: Solid State Science and Technology, 112, No. 12, p. 1666 (1975). When a silicon chloride gas system is used, the growth of the polycrystalline region 30 over silicon dioxide can be reduced by controlling the concentration of HCl in the system.

The silicon layer 26 is exposed in the next step to an etching solution which etches the polycrystalline region 30 at a faster rate than the monocrystalline regions 28. During this etching step the polycrystalline region 30 is removed while the monocrystalline region 28 remains, as shown in Fig. 5. One etching solution which can be used to remove the polycrystalline region 30 is buffered HF, or NF_4F:HF, in a ratio between 1:5 and 1:10. The buffered HF filters through the relatively porous polycrystalline region 30 and attacks the surface of the silicon dioxide layer 16, causing the polycrystalline region 30 to lift off, or peel off, the surface. No such effect occurs in the monocrystalline regions 28. An alternative mixture, which operates by selective etching rather than lift-off, is potassium hydroxide and n-propanol. In selective etching, the polycrystalline region 30 is etched at a higher rate than the monocrystalline regions 28. Another selective etching mixture is ethylenediamine, catechol and water. One suitable example of this mixture is 46.4 mole % ethylenediame, 4.2 mole % catechol, and 49.4 mole % water and an etching temperature of about 80°C is used.

After the polycrystalline region 30 of the silicon layer 26 has been removed, a second oxide layer 32 is grown over the surface of the semiconductor wafer 10 as shown in Fig. 6. In reality, the oxide layer 32 is a continuation of the growth of the oxide layer 16. However, the oxide layer 32 is separately identified in Fig. 6 for purposes of clarity. The oxide layer 32 does not grow over the silicon nitride layer 22 but lifts the edges of the silicon nitride layer 22 by a small amount as is known in the art. To avoid impurity redistribution in the semiconductor wafer 10, a low temperature, high-pressure oxidation process is utilized. Typically, a temperature of about 950°C and a pressure of about 10 atmospheres are used for growth of the oxide layer 32.

The silicon nitride layer 22 is then stripped off the wafer 10 to provide access to the source window 20, as shown in Fig. 7. The silicon nitride layer 22 can be removed by known methods such as exposure to phosphoric acid at about 80°C or plasma etching. In this step, the oxide layers 16 and 32 are left intact. Next, a thin source electrode 34 is formed by ion implanation or diffusion of impurities. In the static induction transistor, the source lectrode 34 has low resistivity and is of the same conductivity type as the epitaxial layer 12.

A partial top view of the semiconductor wafer 10 is shown in Fig. 8. The monocrystalline regions 28 which cover the gate electrodes 24 are in the form of elongated strips and are buried under the oxide layer 32. The monocrystalline regions 28 include enlarged portions 36 at one end thereof. In the next step of the process of the present invention, gate contact windows 38 are opened in the oxide layers over the enlarged portions 36 utilizing the process described hereinabove in connection with the opening of windows 18 and 20. The use of enlarged portions 36 obviates the requirement for precision mask alignment in this step.

In a metallization step, metallic gate and source contacts are deposited and patterned. A gate contact 40 includes fingers 42, which extend over the gate contact windows 38 for making electrical contact to the monocrystalline regions 28, and a relatively large region for external lead attachment. A source contact 42 includes a finger 46, as shown in Figs. 8 and 9, in the source window 20, for making electrical contact to the source electrode 34, and a relatively large region for external lead attachment. The metallic contacts are typically made by sputtering of aluminum including 2% silicon. An appropriate mask produces the metallic contact patterns. While the metallization mask requires reasonably precise alignment to ensure proper placement of the source contact 42, a small misalignment of the source contact 42 does not seriously degrade the performance of the static induction transistor. Mask alignment is also less critical with respect to the gate contact 40 since the device dimensions are larger in the region of the gate contact windows 38 than in the elongated strip portions of the monocrystalline regions 28.

It is to be understood that Figs. 1–9 illustrate only a portion of the semiconductor wafer 10. A complete static induction transistor typically includes multiple source electrodes in an array of parallel strips. Parallel gate electrodes are located between each pair of source electrodes. The source electrodes and gate electrodes, respectively, are con-

nected in parallel to form a device with the desired power handling capability.

The completed SIT with low capacitance self-aligned gate electrodes is illustrated in Figs. 8 and 9. An ohmic contact 48 is attached to the bottom surface of the substrate 14 and constitutes the drain contact for the device. By way of specific example, a high frequency SIT can be fabricated with the substrate 14 having a resistivity of about .01 ohm centimeter, the high resistivity layer 12 having a resistivity of at least 30 ohm centimeters, the gate electrodes 24 having an impurity surface concentration of $10^{18}cm^{-3}$, the monocrystalline regions 28 having a resistivity of less than 0.1 ohm centimeters, and the source electrode having a resistivity of less than 0.1 ohm centimeter. Gate and source electrodes are typically 1.5 to 2.5 microns in width and are spaced apart by 4 to 5 microns. Gate and source electrode depths are typically 2.5 to 3 microns and 0.3 microns, respectively. Further details regarding the construction and operation of static induction transistors are disclosed by Nishizawa et al in U.S. Patent Nos. 3,828,230 and 4,199,771; by Nishizawa et al in "Field Effect Transistor Versus Analog Transistor (Static Induction Transistor)," *IEEE Transactions on Electron Devices*, Vol. ED-22, No. 4, April 1975; and Nishizawa et al in "High Frequency High Power Static Induction Transistor," *IEEE Transactions on Electron Devices*, Vol. ED-25, No. 3, March 1978.

In an alternative approach, the source contact is formed as a monocrystalline silicon region over the source electrode, as shown in Figs. 10 and 11. The device is fabricated in the manner described hereinabove up to and including the step of stripping the silicon nitride layer 22. Then a second silicon layer, having the same condutivity type as the epitaxial layer 12 but having very low resistivity, is grown over the semiconductor wafer 10, as described hereinabove in connection with the silicon layer 26. The second silicon layer inludes a monocrystalline region 50 over the source electrode 34 and a polycrystalline region (not shown) over the remainder of the semiconductor wafer 10. The second silicon layer is then exposed to an etching solution which removes the polycrystalline region but does not attack the monocrystalline region 50. Suitable etching solutions are described hereinabove. After etching of the second silicon layer, a protective oxide layer 52 is grown over the semiconductor wafer 10. During the oxidation step, the source electrode 34 is formed by outdiffusion from the highly doped region 50.

The monocrystalline region 50 which covers the source electrode 34 includes an enlarged portion 54 at one end thereof as illustrated in Fig. 11. Gate contact windows 38 and source contact windows 56 are opened in the oxide layers over the enlarged portions 36 and 54, respectively, utilizing the process described hereinabove in connection with the opening of windows 18 and 20. Because of the relatively large dimensions of the enlarged portions 36 and 54, precision mask alignment is not required.

A metallic gate contact 40 includes fingers 42, which make electrical contact to the monocrystalline regions 28, and a larger region for lead attachment, as described hereinabove. A metallic source contact 58 includes a finger 60, which extends over the source contact window 56 for making electrical contact to the monocrystalline region 50, and a larger region for lead attachment. The contacts 40 and 58 are made by sputtering of aluminum including 2% silicon. An appropriate mask produces the metallic contact patterns. Since the metallic contacts are aligned only with the enlarged portions 36 and 54, precision alignment of the metallization mask is not required.

The completed SIT with low capacitance self-aligned gate and source electrodes, as illustrated in Figs. 10 and 11, can have the parameters of the device shown in Figs. 8 and 9 and described hereinabove. The monocrystalline region 50 can have a resistivity of less than 0.1 ohm centimeter.

Thus, there is provided by the present invention an electrode structure in which the parasitic capacitance associated with metallic contact window overlap is reduced. The reduction in contact window overlap by metallic contacts results in a significant reduction in parasitic capacitance and an improvement in high frequency device performance. Furthermore, there is provided a method for fabricating closely spaced electrodes in a high frequency semiconductor device while avoiding the requirement for precision mask alignment and mask to mask registration.

While there has been shown and described what it at present considered the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

CLAIMS

1. A method for forming self-aligned first and second electrodes in a semiconductor device while avoiding the requirement for precision mask alignment and mask registration, said method comprising the steps of:

growing a first oxide layer on a silicon semiconductor wafer in which said first and second electrodes are to be formed;

opening first and second windows in said first oxide layer;

depositing a protective silicon nitride layer in said first window;

doping said semiconductor wafer through said second window thereby forming said second electrode;

growing a silicon layer of the same conductivity type as said second electrode over said wafer, said silicon layer growing as a low resistivity monocrystalline region over said second electrode and as a polycrystalline region over the remainder of said wafer;

exposing said wafer to a first etching solution which removes said polycrystalline region but which has little effect on said monocrystalline region;

growing a second oxide layer on said wafer in a low temperature, high-pressure process;

exposing said wafer to a second etching solution which removes said silicon nitride layer from said first window without affecting said oxide layers;

doping said semiconductor wafer through said first window thereby forming said first electrode;

opening a contact window through said second oxide layer to an enlarged portion of said monocrystalline region; and

depositing and patterning metal oversaid contact window and said first electrode for making electrical contact to said first and second electrodes.

2. The method as defined in claim 1 wherein said silicon layer is grown in an epitaxial reactor by chemical vapor deposition.

3. The method as defined in claim 2 wherein said silicon layer is grown at a temperature between about 950°C and 1000°C.

4. The method as defined in claim 2 wherein said doping through said first and second windows includes forming of said first and second electrodes by diffusion.

5. The method as defined in claim 2 wherein said doping through said first and second windows includes forming of said first and second electrodes by ion impantation.

6. The method as defined in claim 2 wherein said first etching solution includes NH_4F:HF in a ratio between 1:5 and 1:10, said first etching solution being operative to lift said polycrystalline region off said wafer.

7. The method as defined in claim 2 wherein said first etching solution includes potassuim hydroxide and n-propanol.

8. The method as defined in claim 2 wherein said first etching solution includes ethylenediamine, catechol, and water.

9. A method for forming self-aligned gate and source electrodes in a static induction transistor while avoiding the requirement for precision mask alignment and mask to mask registration, said method comprising the steps of:

growing a first oxide layer over a high resistivity epitaxial silicon layer on a semiconductor wafer;

opening gate and source windows in said first oxide layer;

depositing a protective silicon nitride layer in said source window;

doping said high resistivity epitaxial silicon layer through said gate window thereby forming said gate electrode;

placing said wafer in an epitaxial reactor in which a low resistivity silicon layer of the same conductivity type as said gate electrode is grown over said wafer, said low resistivity silicon layer growing as a monocrystalline region over said gate electrode and as a polycrystalline region over said first oxide layer and said silicon nitride layer;

exposing said wafer to a first etching solution which removes said polycrystalline region but which has little effect on said monocrystalline region;

growing a second oxide layer on said wafer under low temperature, high-pressure conditions;

exposing said wafer to a second etching solution which removes said silicon nitride layer from said source window without affecting said oxide layers;

doping said high resistivity epitaxial silicon layer through said source window thereby forming said source electrode;

opening a gate contact window through said second oxide layer to an enlarged portion of said monocrystalline region; and

depositing and patterning metal over said gate contact window and said source electrode for making electrical contact to said source and gate electrodes.

10. The method as defined in claim 9 wherein said low resistivity silicon layer is grown at a temperature between about 950°C and 1000°C.

11. The method as defined in claim 9 wherein said first etching solution includes NH_4F:HF in a ratio between1:5 and 1:10, said first etching solution being operative to lift said polycrystalline region off said wafer.

12. The method as defined in claim 9 wherein said monocrystalline region is between 0.5 and 1.5 microns in thickness.

13. A method for forming self-aligned first and second electrodes in a semiconductor device while avoiding the requirement for precision mask alignment and mask to mask registration, said method comprising the steps of:

growing a first oxide layer on a silicon semiconductor wafer in which said first and second electrodes are to be formed;

opening first and second windows in said first oxide layer;

depositing a protective silicon nitride layer in said first window;

doping said semiconductor wafer through said second window thereby forming said second electrode;

growing a first silicon layer of the same conductivity type as said second electrode over said wafer, said first silicon layer growing

as a low resistivity monocrystalline region over said second electrode and as a first polycrystalline region over the remainder of said wafer;

exposing said wafer to a first etching solution which removes said first polycrystalline region but which has little effect on said monocrystalline region over said second electrode;

growing a second oxide layer on said wafer in a low temperature, high-pressure process;

exposing said wafer to a second etching solution which removes said silicon nitride layer from said first window without affecting said oxide layers;

growing a second silicon layer of the same conductivity type as said first electrode over said wafer, said first silicon layer growing as a low resistivity monocrystalline region over said first electrode and as a second polycrystalline region over the remainder of said wafer;

exposing said wafer to the first etching solution which removes said second polycrystalline region but which has little effect on said monocrystalline region over said first electrode;

gorowing a third oxide layer on said wafer in a low temperature, high-pressure process;

opening a first electrode contact window through said third oxide layer to an enlarged portion of said monocrystalline region over said first electrode and opening a second electrode contact through said second and third oxide layers to an enlarged portion of said monocrystalline region over said second electrode; and

depositing and patterning metal over said contact windows for making electrical contact to said first and second electrodes.

14. A field effect semiconductor device having low parasitic capacitance, said device comprising:

a high resistivity layer of semiconductor material of one conductivity type;

a low resistivity source electrode formed on a first surface of said high resistivity layer;

a low resistivity drain electrode formed on a second surface of said high resistivity layer;

low resistivity gate electrodes of the opposite conductivity type formed on the first surface of said high resistivity layer on opposite sides of said source electrode; and

very low resistivity monocrystalline silicon gate contacts disposed on said gate electrodes without overlap thereof, said gate contacts having the same conductivity type as said gate electrodes and including enlarged portions to which electrical contact is made by a gate metallization,

whereby the parasitic capacitance associated with metallic gate contact overlap is eliminated.

15. The field effect semiconductor device as defined in claim 14 further including a very low resistivity monocrystalline silicon source contact disposed on said source electrode without overlap thereof, said source contact having the same conductivity type as said source electrode and including an enlarged portion to which electrical contact is made by a source metallization,

whereby the parasitic capacitance associated with metallic source contact overlap is eliminated.

16. The field effect semiconductor device as defined in claim 15 wherein said gate and source contacts are between about 0.5 and 1.5 microns in thickness.

17. The field effect semiconductor device as defined in claim 14 wherein said gate and source electrodes have the form of parallel strips in the first surface of said gate contacts are located at one end of said parallel strips.

18. A method of forming a self-aligned semiconductor electrode structure, substantially as described herein with reference to the accompanying drawings.

19. A field effect semiconductor device, substantially as described herein with reference to the accompanying drawings.

20. The features herein described, or their equivalents, in any novel selection.

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